REMARKS

Applicants appreciate the detailed examination evidenced by the Official Action mailed June 12, 2007 (hereinafter the "Official Action"). In response, Applicants have canceled Claims 1-5 and have added new claims 6-14 including new independent Claims 6 and 10.

Applicants respectfully submit that the cited art does not disclose or suggest the recitations of, for example, independent Claims 6 and 10, which specify that the number of rows and columns included in the MRAM is increased by increasing the reverse bias resistance (of magnetic memory cells). Further, the cited art does not disclose or suggest that the number of cells is limited according to the relation of:

$$\eta = \sqrt{\frac{R_m * \varepsilon(2+K_{DR})}{R_r(1-\varepsilon)}},$$

as recited in dependent Claims 7 and 11. Accordingly, Applicants respectfully submit that all claims are patentable for at least the reasons described herein.

The Objections and Rejections Have Been Overcome by Amendment

Claims 1 and 3-4 stand objected to. *Official Action, p. 2.* Applicants have canceled these claims without prejudice or disclaimer thereby rendering these objections moot. Applicants have also canceled Claim 2, the recitations of which form the basis for the objections to the specification as set out in the Official Action at p. 2. As shown above, Claim 2 has also been canceled herein by amendment, thereby rendering the present objection moot.

Independent Claims 6 and 10 are Patentable Over Scheuerlein and Sharma

Claims 1-2 and 4 stand rejected under 35 U.S.C. § 103 over U.S. Patent No. 6, 130, 835 to Scheuerlein ("Scheuerlein") in view of U.S. Patent No. 6,885,573 to Sharma et al. ("Sharma"). *Official Action, p. 2.* Applicants acknowledge that Scheuerlein and Sharma both discuss the inclusion of diodes in MRAM arrays. However, Scheuerlein and Sharma (either

singly or in combination) do not disclose or suggest the detailed recitations of the new independent claims.

For example, new Claim 6 recites in part:

> an array of magnetic memory cells arranged in intersecting rows and columns, wherein each of the magnetic memory cells comprises a cell resistance;
>
> a plurality of magnetic memory cell selection devices, each of which is coupled to a respective one of the magnetic memory cells in the array to enable selective access to any of the magnetic memory cells during a write operation, wherein each of the selection devices comprises a reverse bias resistance,
>
> wherein a number of the rows and columns is increased by increasing the reverse bias resistance.

Although Scheuerlein does discuss inclusion of diodes in MRAM arrays, the object of Scheuerlein appears to be limited to reducing leakage current. For example, one of the exemplary portions of Scheuerlein reads as follows:

> The present invention provides a nonvolatile cross point memory array having memory cells that are capable of operating at voltages and power levels that are suitable for integration using deep sub-micron VLSI technologies. The present invention also provides a memory cell having a birdirectionally conducting nonlinear resistance cell selection device **providing a low power cross point memory array than conventional cross point memory arrays**. The MR memory cell of the present invention has operating biasing points that provide a reduced voltage swing required for selecting a bit line so that sensing times are thereby shorter than conventional MR memory cells. *(emphasis added).*

Scheuerlein, Col. 3, ll. 10-22. Scheuerlein further states that:

> What is needed is a nonvolatile cross point memory array having memory cells that are capable of operating at voltages and power levels that are suitable for integration using deep sub-micron VLSI technologies. What is also needed is a memory cell having a cell selection device providing a low series resistance and a low voltage biasing, **thereby providing a low power cross point memory array than conventional cross point memory arrays.** Further, what is needed is an MR memory cell having operating biasing points providing a reduced voltage swing required for selecting a bit line so that sensing times are thereby shorter than conventional MR memory cells. Further still, what is needed is a cross point memory array that uses a bias level that minimizes power dissipation in the array *(emphasis added).*

Scheuerlein, Col. 2, l. 61-Col. 3, l. 7.

As shown above by the cited passages of Scheuerlein, the discussion therein focuses in large part on the benefits of including diodes in the cross-point array which leads to the objective of reduced power. However, there is nothing in Scheuerlein which discloses or suggests how a maximum number of rows and columns can be provided in a square MRAM array based on the inclusion of diodes as selection circuits.

Sharma also relates to the use of diodes in MRAM arrays. In particular, the objective of Sharma is as follows:

> Accordingly, there is a need to be able to reduce, if not eliminate, leakage current that exists when diodes are utilized. What is further needed is a method of manufacturing an MRAM device having such diodes that reduces costs and improves performance by reducing or eliminating leakage current through the diodes within the device.

Sharma, Col. 2, ll. 15-20.

As shown above by the cited passage of Sharma, the objective therein is, again, to reduce leakage current. Furthermore, the objective of Sharma goes beyond just the mere inclusion of diodes in the array, to focus on minimizing a leakage current through individual diodes included therein. For example, one relevant portion of Sharma reads as follows:

> The use of a large common metal-Si contact area improves the contact resistance at the common cathode. This improves the current density capacity of each diode 88. Since each diode 88 has a separate Pt contact with its associate MRAM cell, each diode 88 is separate from one another. Further, the common metal-Si contact reduces, if not eliminates, current sneak paths or leakage current associated with diodes fabricated using techniques of the prior art.

Sharma, Col. 9, ll. 19-28.

As shown by the above cited passage of Sharma, the focus of the discussion therein is the particular structure of the diodes to reduce the associated leakage current. However, there is nothing in Sharma which discloses or suggests how an MRAM array should be designed to maximize the number of rows and columns using the parameters discussed above and specifically recited in independent Claims 6 and 10.

There is also no motivation or suggestion to combine Sharma and Scheuerlein. Although both relate to reducing leakage current, Scheuerlein takes the approach of providing a specific type of diode (*i.e.*, a camel diode device or planar doped barrier device) to reduce the leakage current that, whereas Sharma takes a different approach of providing a common metal-semiconductor contact on

the word line as part of the diode included with each of the memory cell arrays to reduce the leakage current. Accordingly, the approaches in Scheuerlein and Sharma, although seeking to achieve the same objective, take different approaches.

Furthermore, both approaches appear limited to how the diode is structured. Accordingly, there is no disclosure suggestion of Scheuerlein and Sharma taken together to provide a way of limiting the number of rows and columns is a square array of MRAM cells based on the specific parameters recited in independent Claims 6 and 10. Accordingly, Applicants respectfully submit that independent Claims 6 and 10 are patentable over Scheuerlein and Sharma for at least these reasons. Furthermore, dependent Claims 7-9 and 11-14 are also patentable over the cited combination for at least the reasons described above with reference to independent Claims 6 and 10.

Many of the dependent Claims are Separately patentable

In addition to the reasons described above in reference to independent Claims 6 and 10, many of the dependent claims provide separate bases for patentability. In particular, nothing in Scheuerlein discloses or suggests the detailed relationship developed by the present inventors indicating how the parameters, such as the data write current non-uniformity, resistance of the magnetic memory cells, the resistance of rows or columns of magnetic memory cells, as well as reverse bias resistance of the diodes compared to the resistance of the magnetic memory cells, can be related to determine an upper limit for the number of rows and columns that can be included in a square MRAM array. See, for example, dependent Claim 7, which recites in-part:

> The MRAM according to Claim 6 wherein the number of the rows and columns included in the device is limited according to the relation:

$$\eta = \sqrt{\frac{R_m * \varepsilon\left(2+K_{DR}\right)}{R_r\left(1-\varepsilon\right)}}$$

> where R_m comprises a resistance of one of the magnetic memory cells, ε comprises a maximum current non-uniformity of the array during a write operation, K_{DR} depends on the reverse bias resistance of one of the magnetic memory cell selection devices, and R_r comprises a resistance of a row or column of the magnetic memory cells.

Dependent Claim 11 includes similar recitations. Nothing in the cited art discloses or suggests the detailed types of recitations of the relationship described above to determine the maximum number of rows and columns that can be included in the array due to the inclusion of diodes. Accordingly, dependent Claims 7 and 11 are patentable for at least these additional reasons.

In summary, Applicants have provided new Claims 6-14 to further clarify that the present subject matter. Applicants respectfully request the withdrawal of all rejections and the allowance of all claims in due course. If any formal matters arise, the Examiner is encouraged to contact the undersigned representative at (919) 854-1400 to resolve any remaining formal issues.

Respectfully submitted,

Robert N. Crouse
Registration No. 44,635
Attorney for Applicants

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone: 919/854-1400
Facsimile: 919/854-1401

CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on September 12, 2007.

Kirsten S Carlos